

FIG. 1

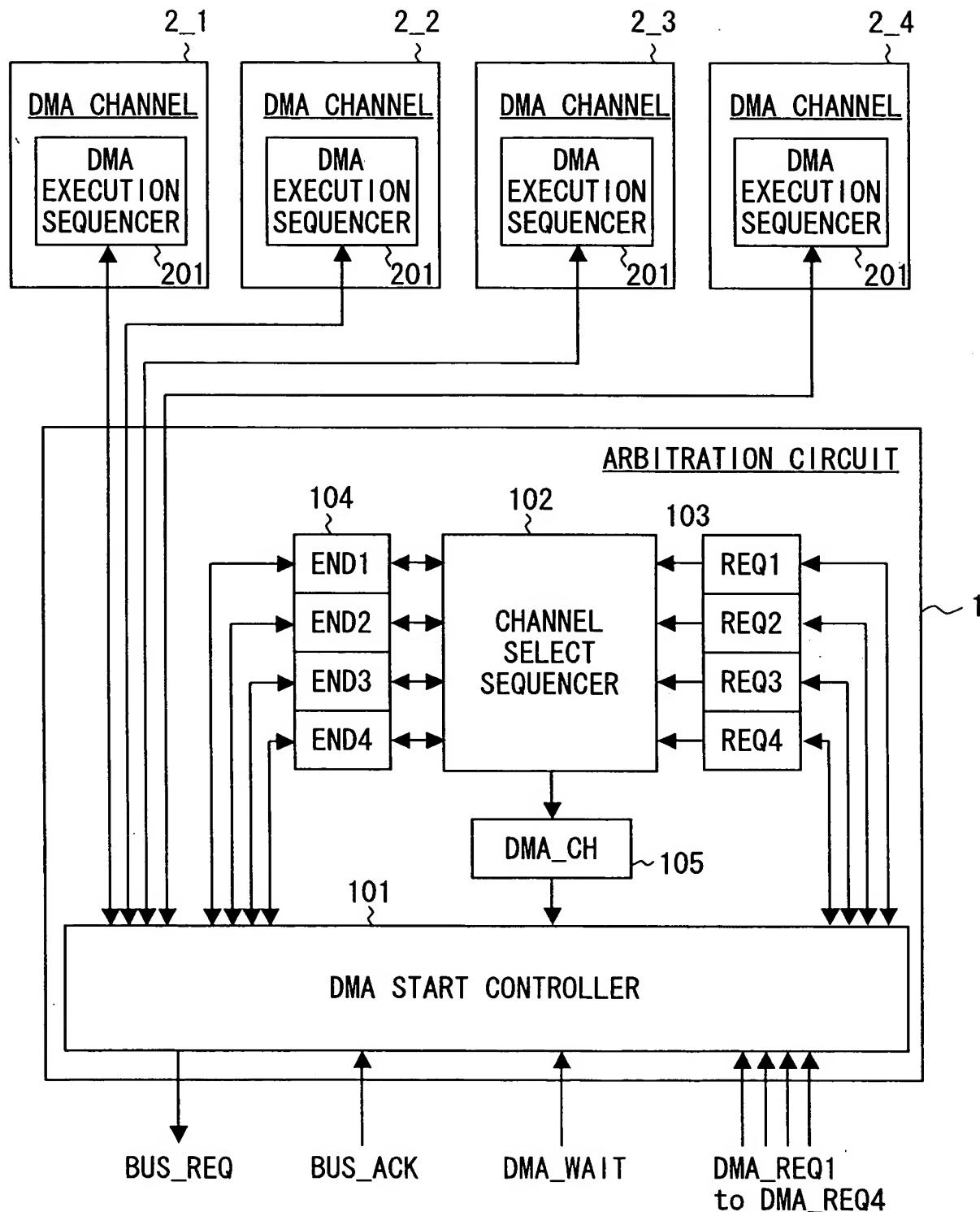


FIG. 2

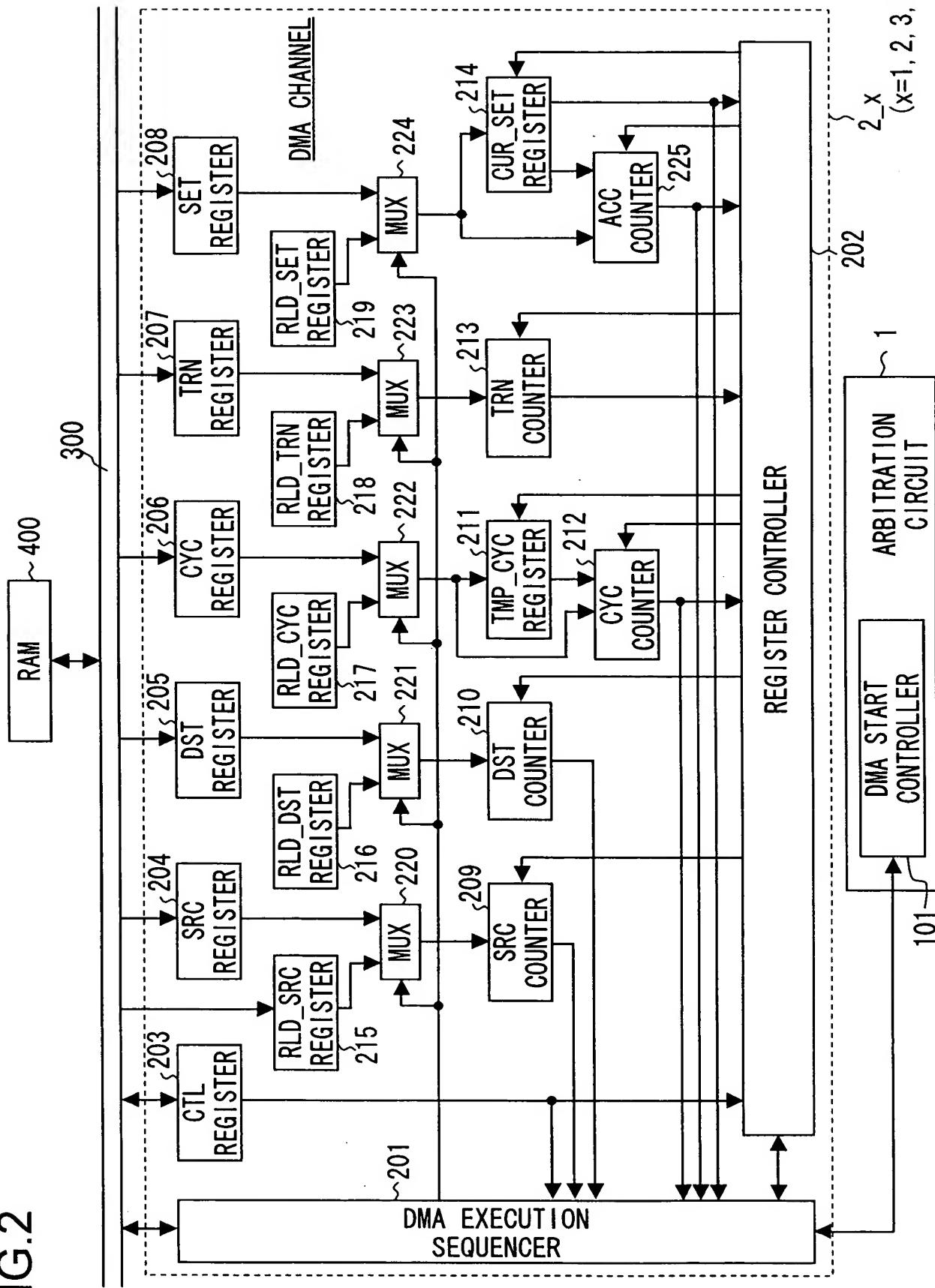


FIG.3

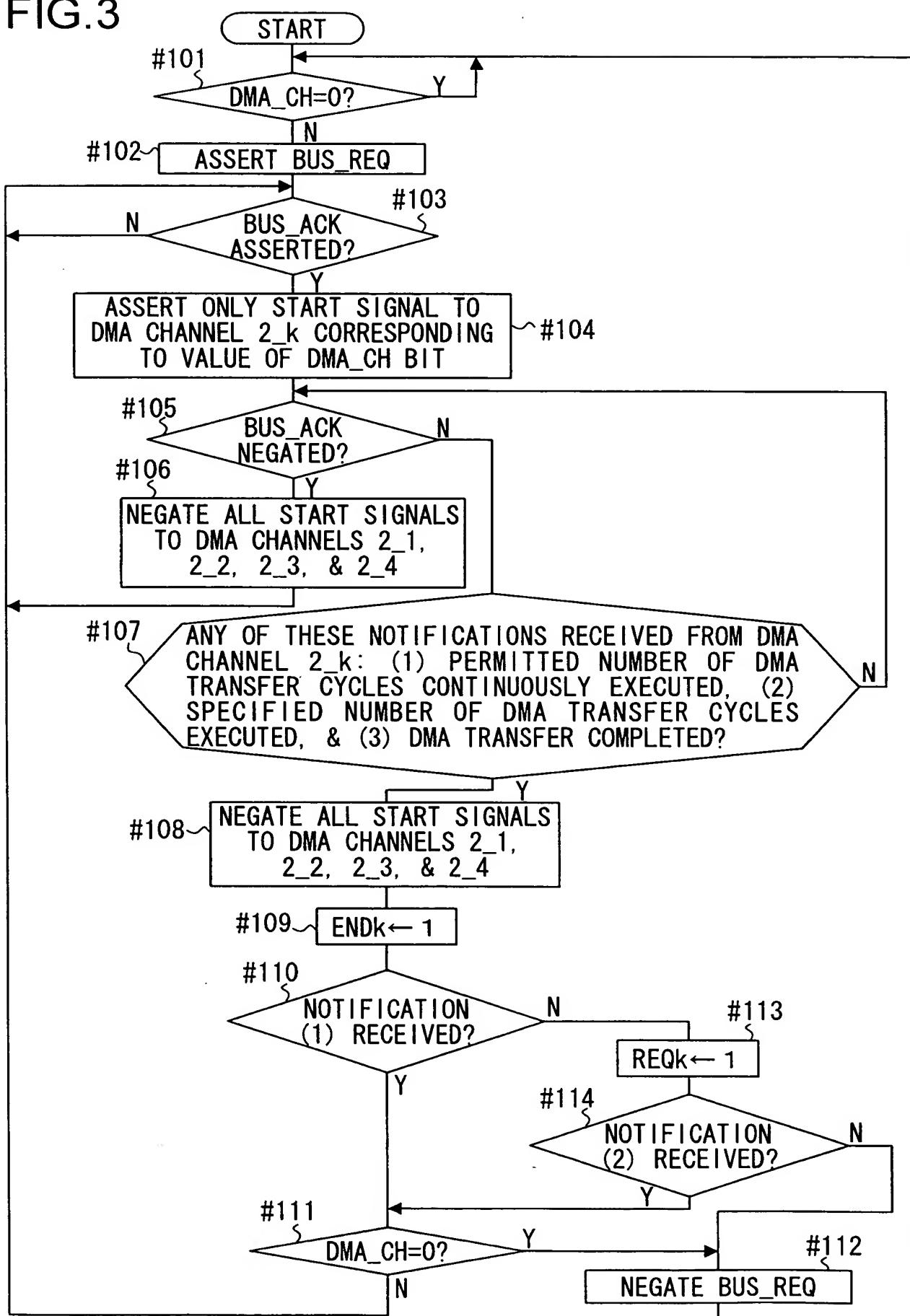


FIG.4

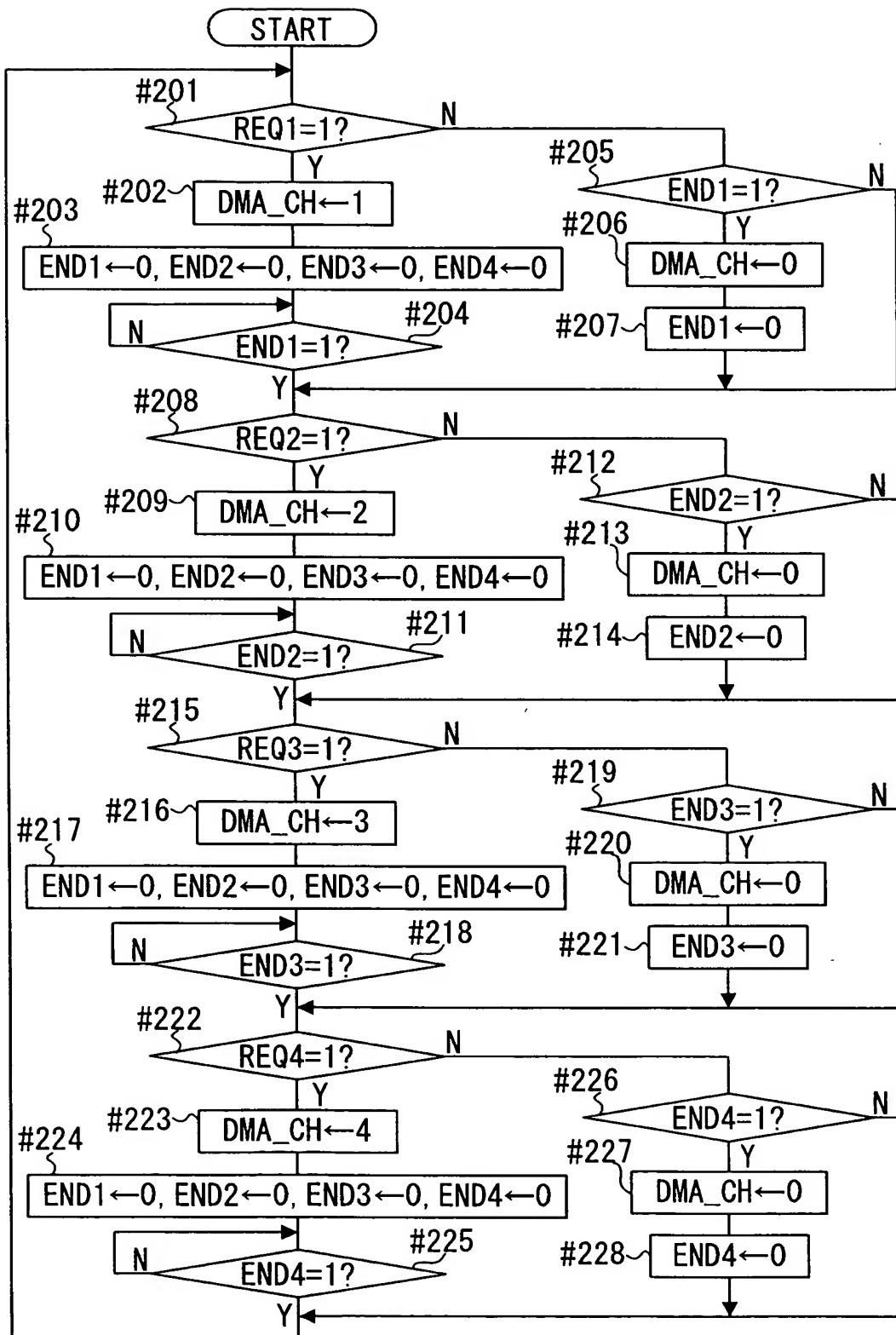


FIG.5

ADDRESS (Hex)	CONTENTS OF DATA
⋮	⋮
20000000-20000003	START ADDRESS (20007774) IN RAM 400 WHERE INFORMATION NEEDED FOR 2ND DMA TRANSFER SESSION IS STORED
20000004-20000007	INFORMATION INDICATING START ADDRESS OF SOURCE IN 1ST DMA TRANSFER SESSION
20000008-2000000B	INFORMATION INDICATING START ADDRESS OF DESTINATION IN 1ST DMA TRANSFER SESSION
2000000C-2000000D	INFORMATION INDICATING NUMBER OF CYCLES INVOLVED IN ONE DMA TRANSFER SESSION IN 1ST DMA TRANSFER SESSION
2000000E-2000000F	INFORMATION INDICATING NUMBER OF DMA TRANSFER SESSIONS TO BE EXECUTED IN 1ST DMA TRANSFER SESSION
20000010-20000011	OTHER INFORMATION RELATING TO 1ST DMA TRANSFER SESSION
20000012	CONTROL INFORMATION RELATING TO 1ST DMA TRANSFER SESSION S/W_START = 0 MOD[1, 0] = [1, 1]
⋮	⋮
20007774-20007777	START ADDRESS (ARBITRARY) IN RAM 400 WHERE INFORMATION NEEDED FOR 3RD DMA TRANSFER SESSION IS STORED
20007778-2000777B	INFORMATION INDICATING START ADDRESS OF SOURCE IN 2ND DMA TRANSFER SESSION
2000777C-2000777F	INFORMATION INDICATING START ADDRESS OF DESTINATION IN 2ND DMA TRANSFER SESSION
20007780-20007781	INFORMATION INDICATING NUMBER OF CYCLES INVOLVED IN ONE DMA TRANSFER SESSION IN 2ND DMA TRANSFER SESSION
20007782-20007783	INFORMATION INDICATING NUMBER OF DMA TRANSFER SESSIONS TO BE EXECUTED IN 2ND DMA TRANSFER SESSION
20007784-20007785	OTHER INFORMATION RELATING TO 2ND DMA TRANSFER SESSION
20007786	CONTROL INFORMATION RELATING TO 2ND DMA TRANSFER SESSION S/W_START = 0 MOD[1, 0] = [1, 0]
⋮	⋮

FIG.6

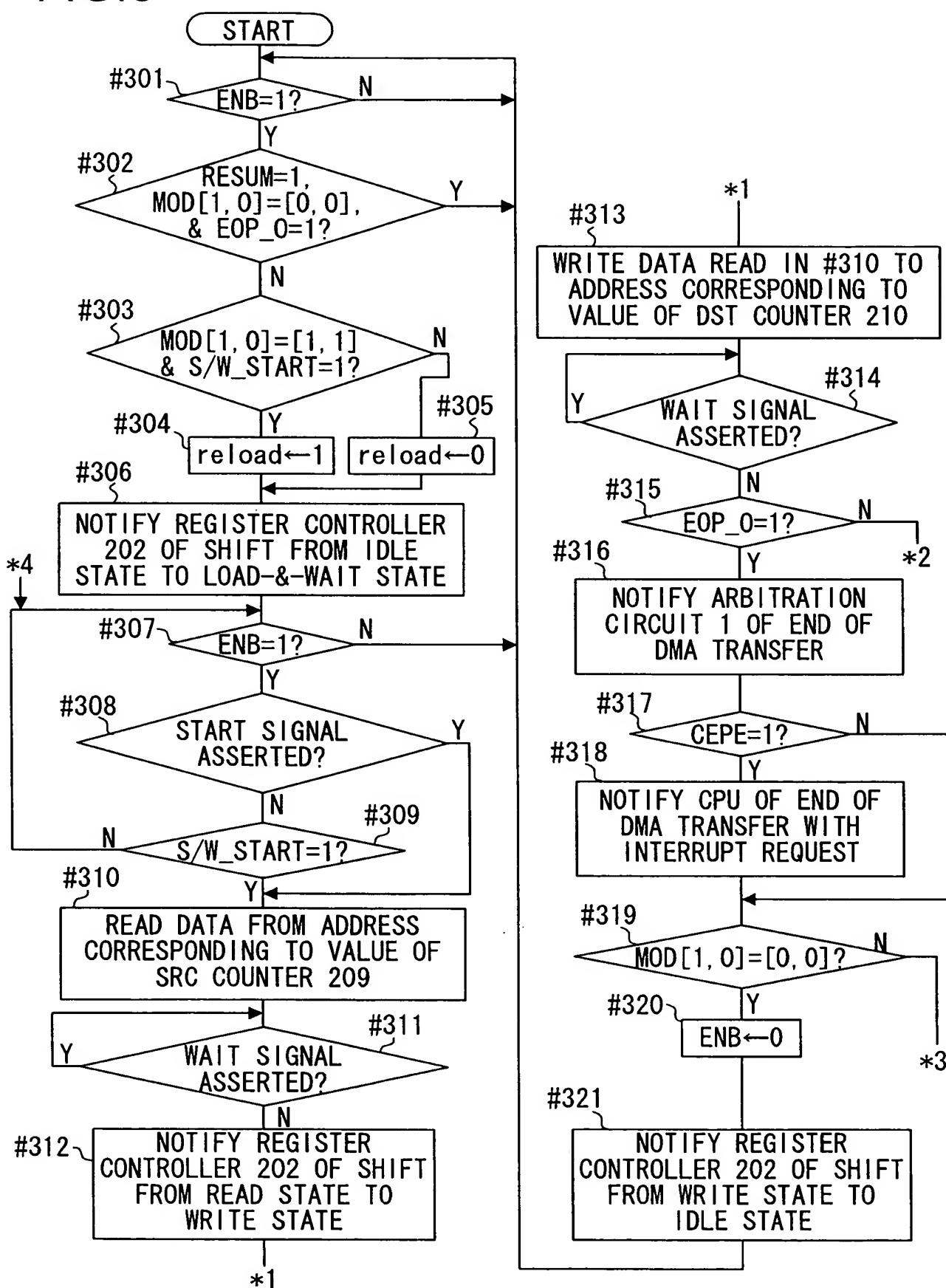


FIG.7

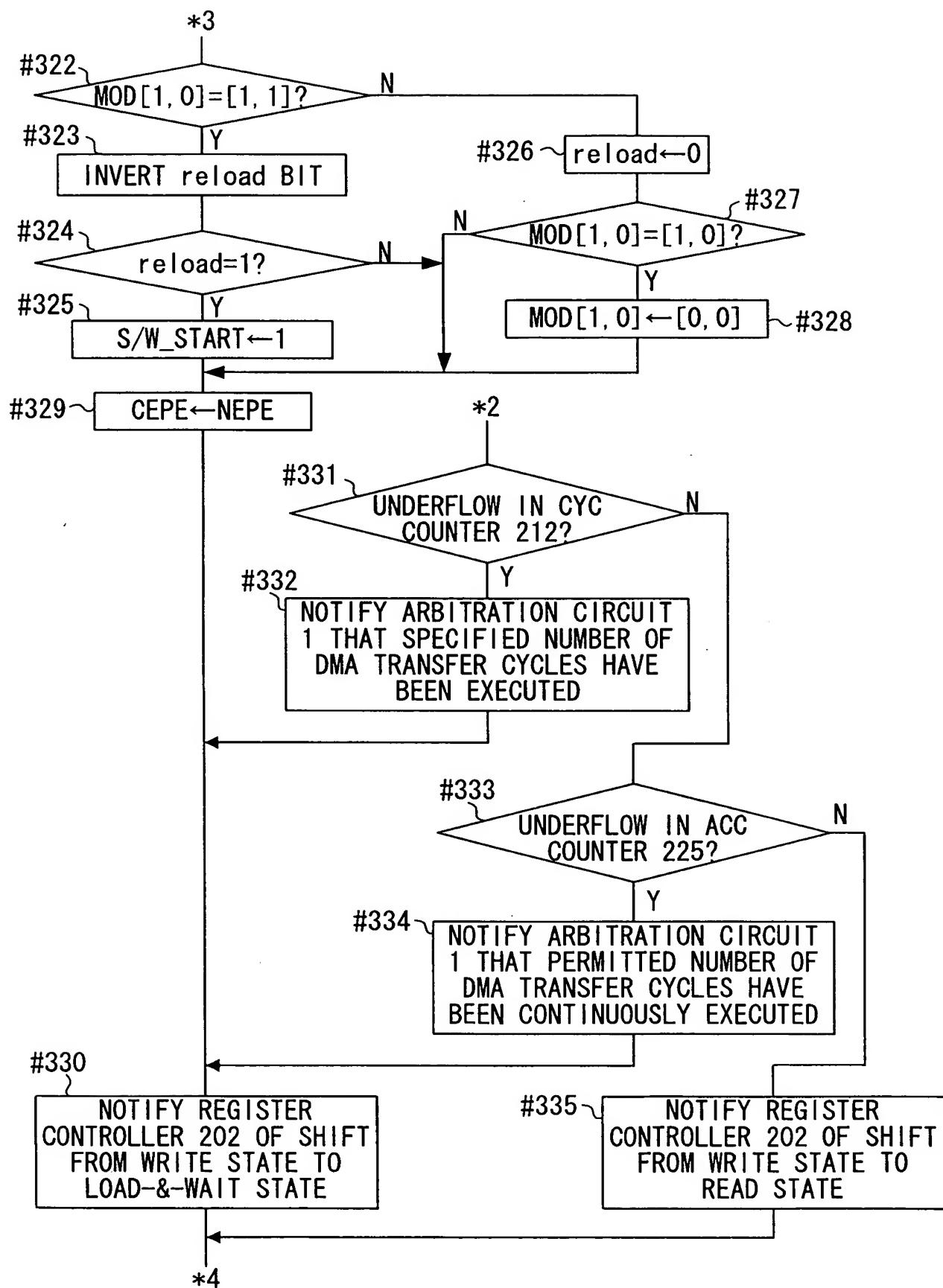


FIG.8

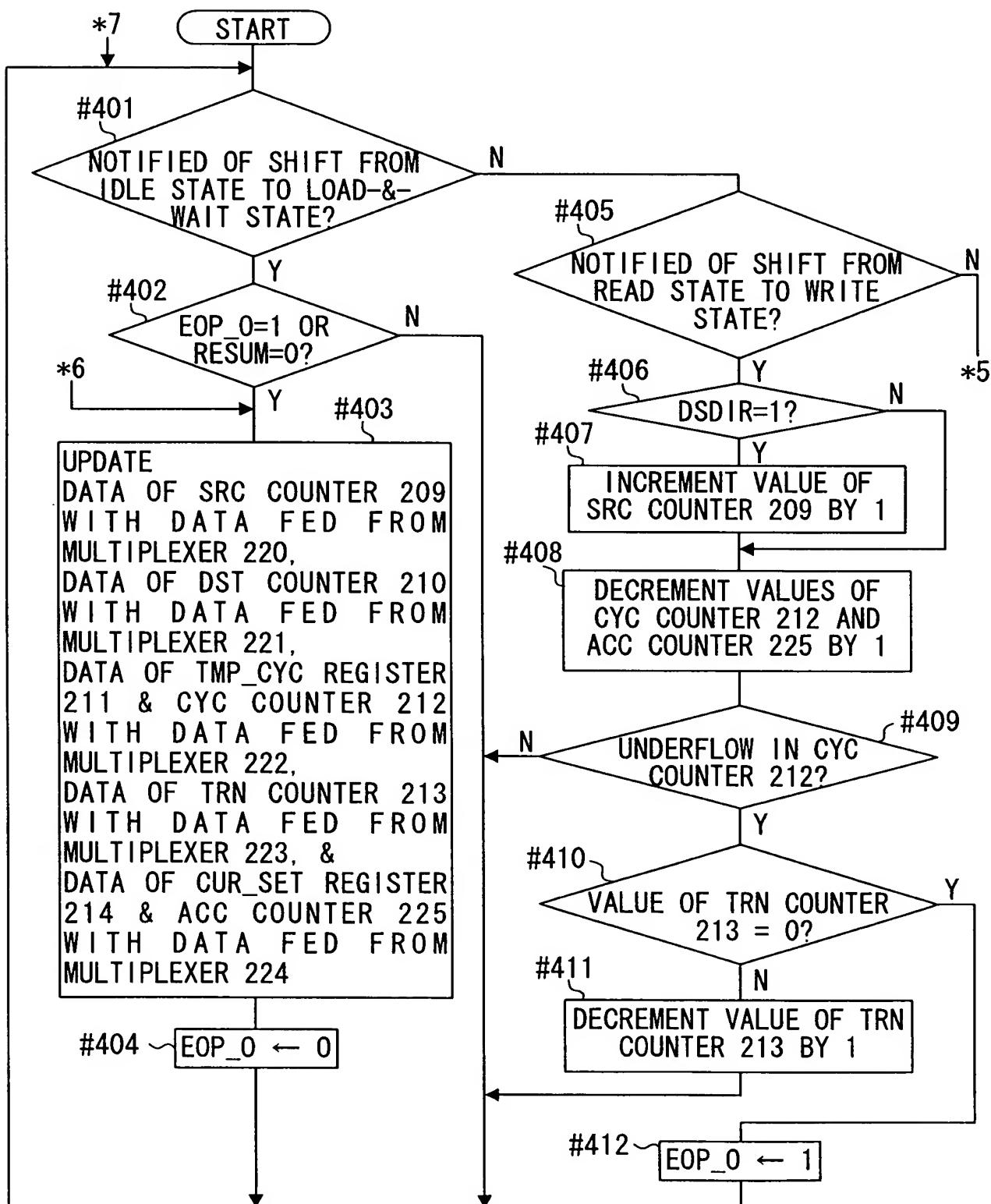


FIG.9

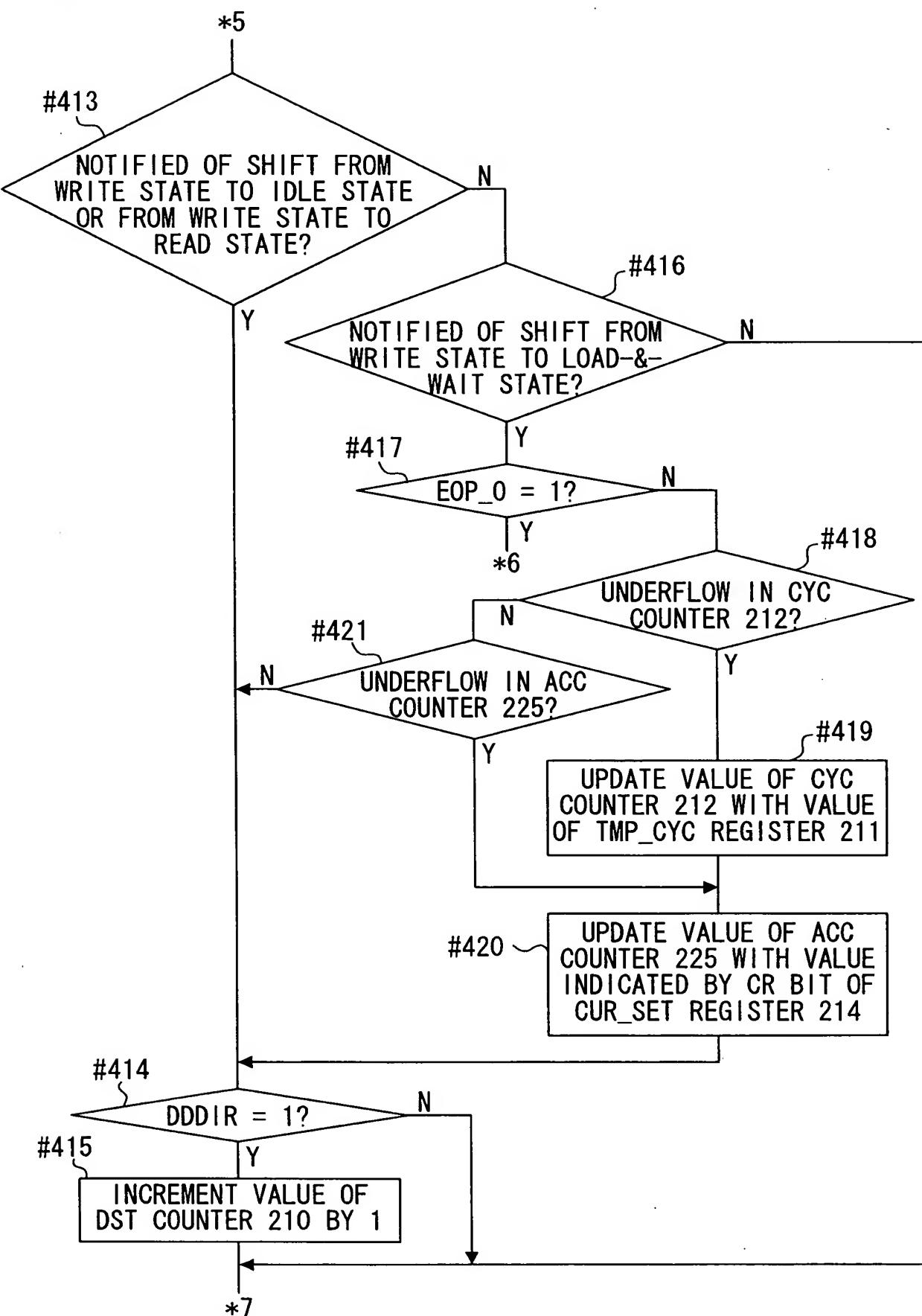


FIG.10

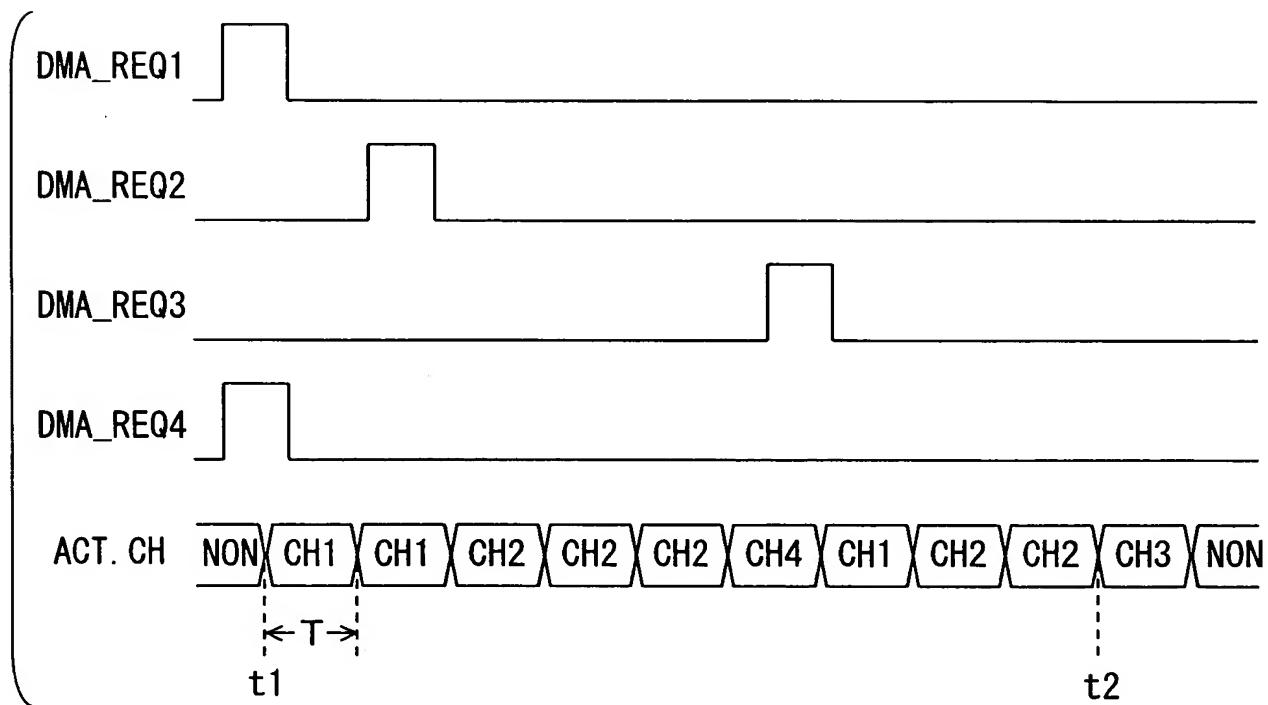


FIG.11A PRIOR ART

PRIORITY	CHANNEL
1	CH2
2	CH3
3	CH4
4	CH1

FIG.11B PRIOR ART

PRIORITY	CHANNEL
1	CH3
2	CH4
3	CH1
4	CH2

FIG.11C PRIOR ART

PRIORITY	CHANNEL
1	CH4
2	CH1
3	CH2
4	CH3

FIG.11D PRIOR ART

PRIORITY	CHANNEL
1	CH1
2	CH2
3	CH3
4	CH4

FIG.12

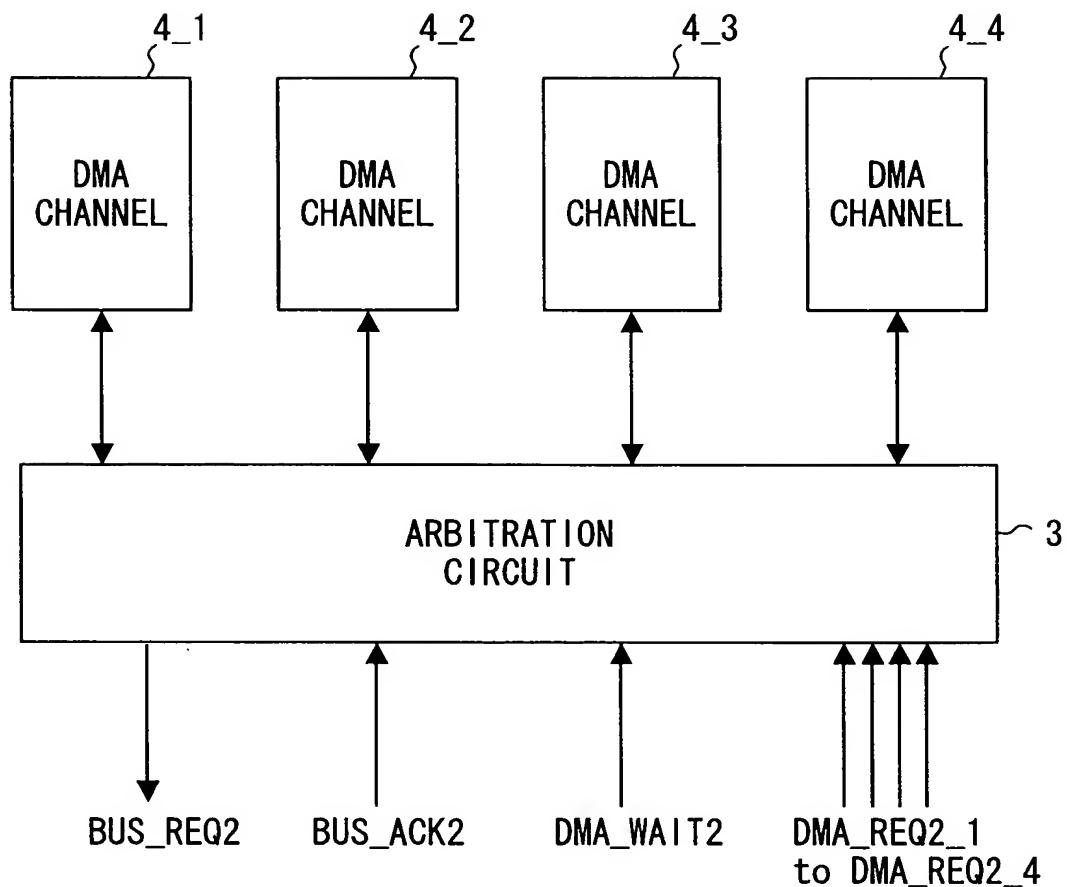


FIG.13

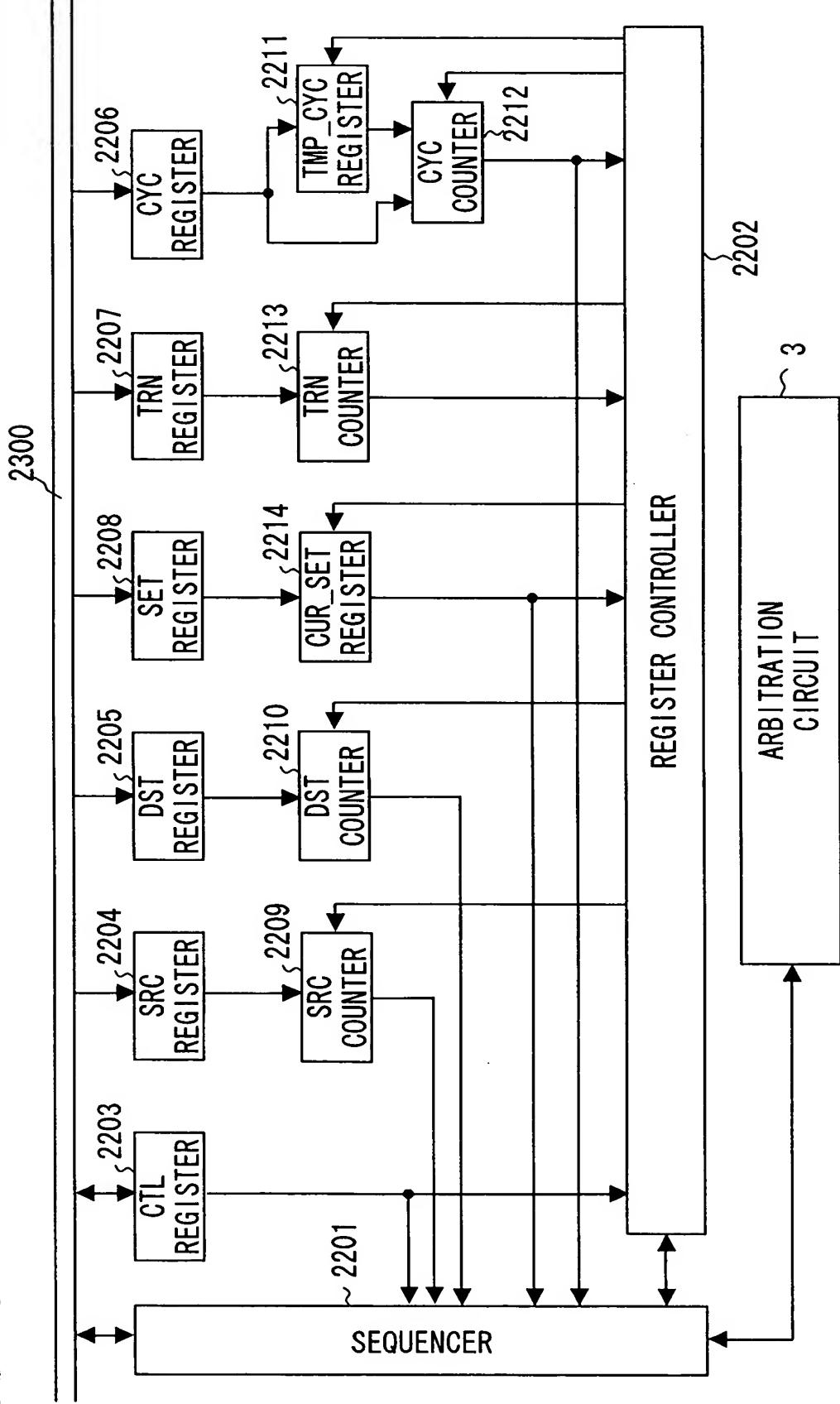


FIG. 14

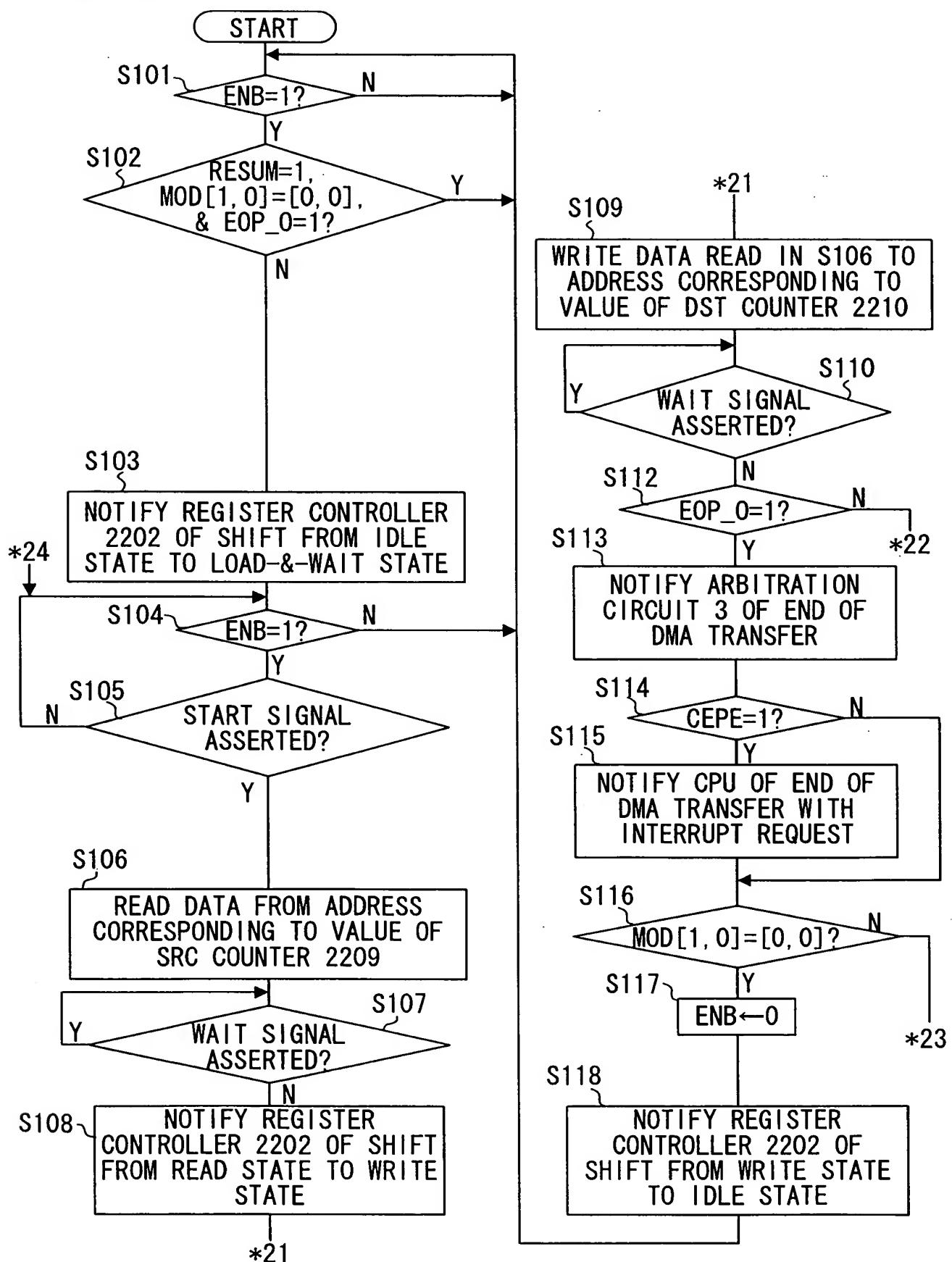


FIG.15

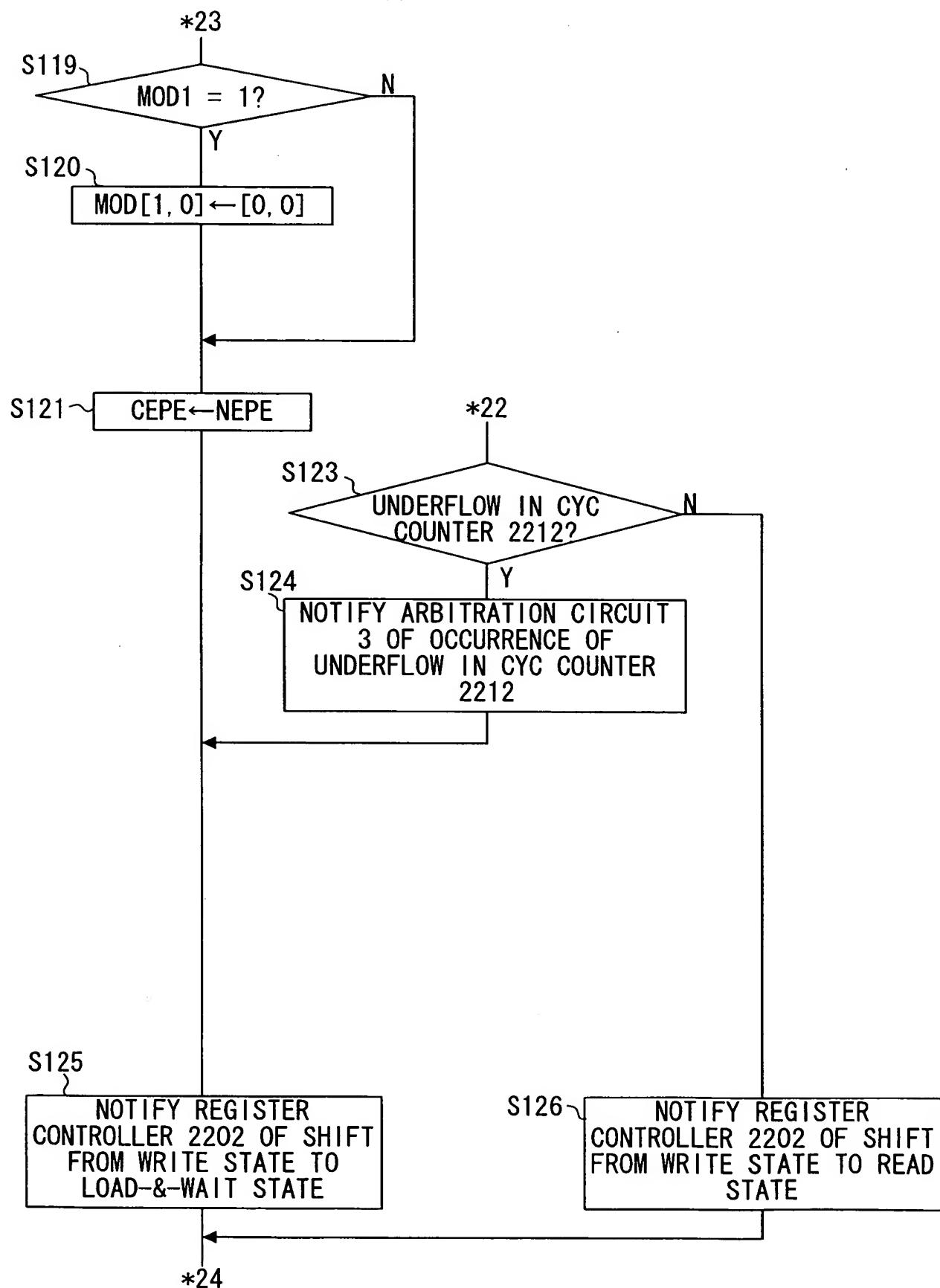


FIG. 16

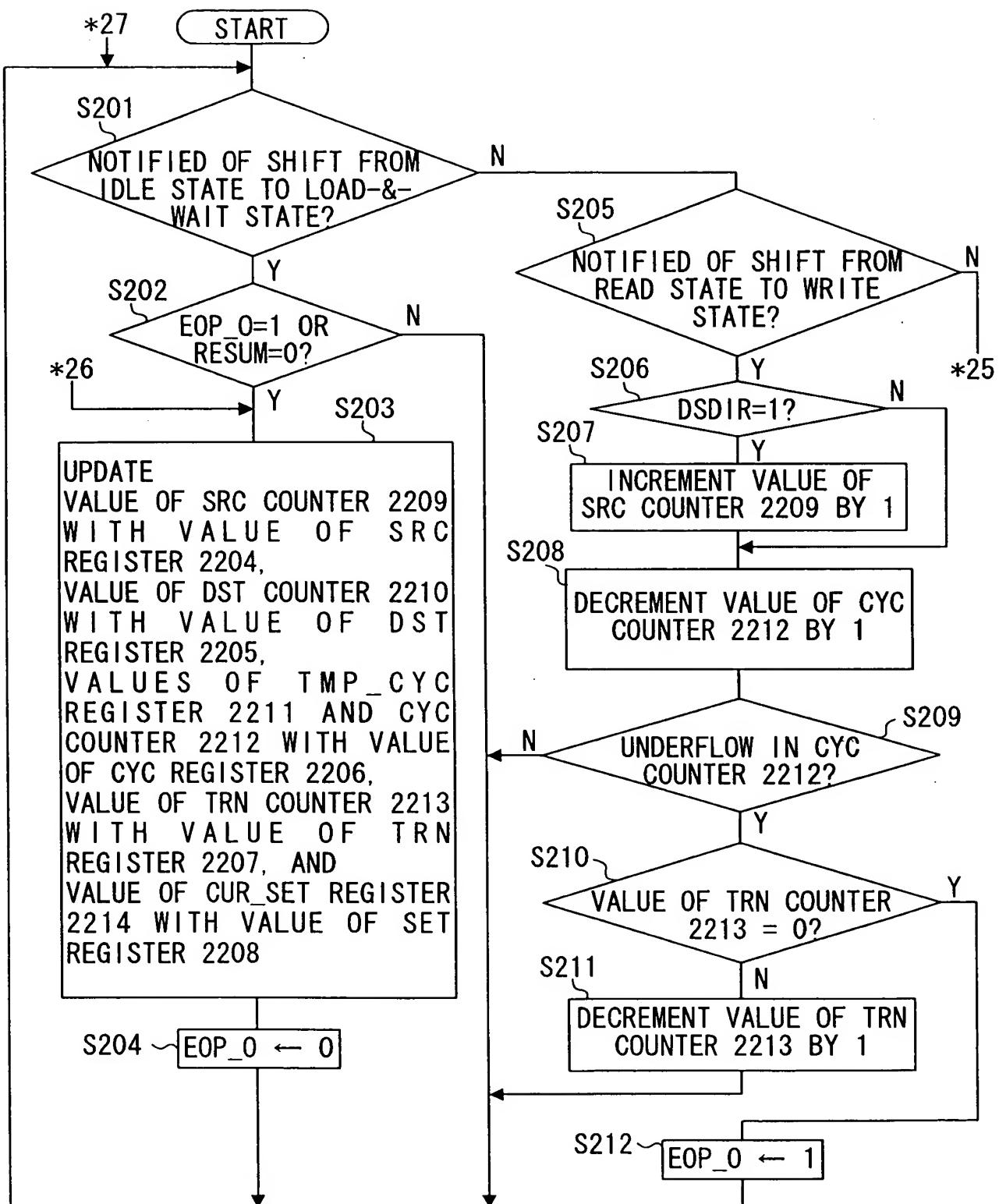


FIG.17

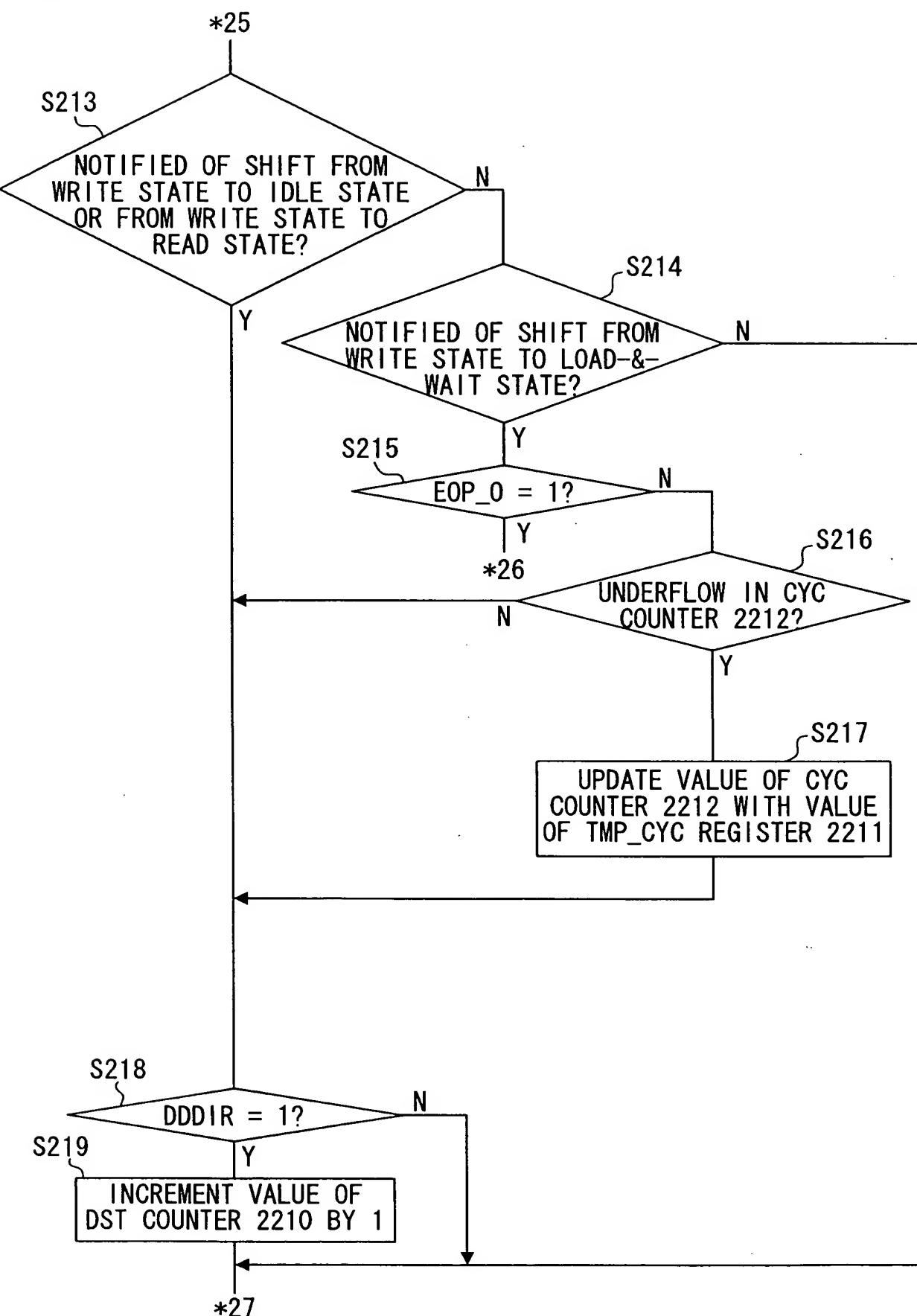
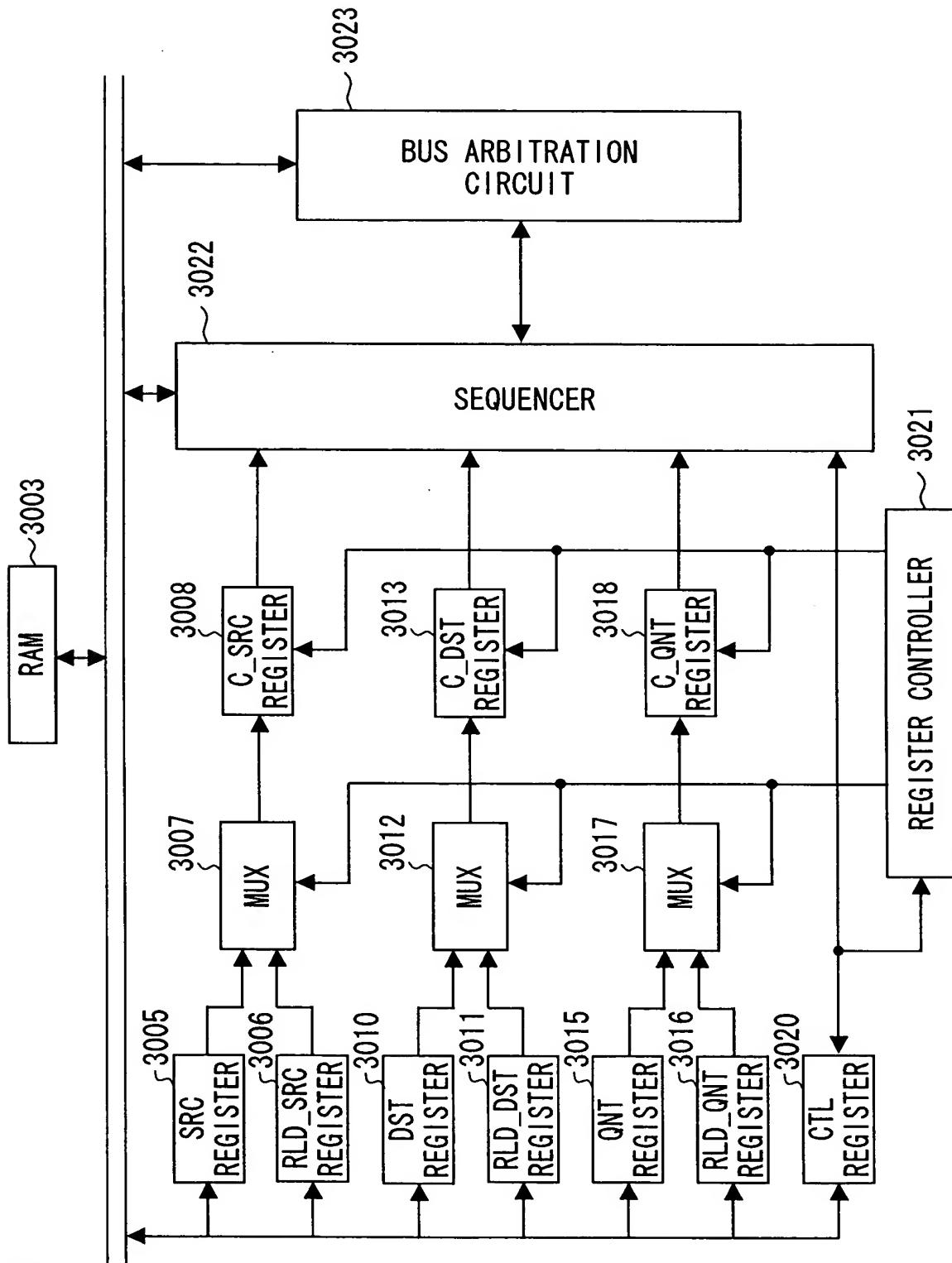


FIG. 18



Title: DATA PROCESSING CONTROL
 APPARATUS AND DMA CONTROLLER
 Inventor: MIURA, et al.
 Appln. No.: Unknown
 Docket No.: 103213-00057

FIG.19

ADDRESS (Hex)	VALUE
1000	2000 (Hex)
1001	SA1
1002	DA1
1003	BYTE1
1004	ENB BIT=1, RLD_ENB BIT=1
.	.
.	.
2000	ARBITRARY
2001	SA2
2002	DA2
2003	BYTE2
2004	ENB BIT=1, RLD_ENB BIT=0

FIG.20

ENB BIT	RLD_ENB BIT	PREVIOUS OPERATION	REGISTERS SELECTED BY MULTIPLEXERS 7, 12, &17	OPERATION
0	ARBITRARY	ARBITRARY	ARBITRARY	NO OPERATION
1	0	ARBITRARY	SRC REGISTER 3005 DST REGISTER 3010 QNT REGISTER 3015	NORMAL DMA TRANSFER
1	1	NORMAL DMA TRANSFER	RLD_SRC REGISTER 3006 RLD_DST REGISTER 3011 RLD_QNT REGISTER 3016	RELOAD
		RELOAD	SRC REGISTER 3005 DST REGISTER 3010 QNT REGISTER 3015	NORMAL DMA TRANSFER

FIG.21

	(1)	(2)	(3)
SRC REGISTER 3005	ARBITRARY	SA1	SA2
RLD_SRC REGISTER 3006	1000 (Hex)	2000 (Hex)	ARBITRARY
DST REGISTER 3010	ARBITRARY	DA1	DA2
RLD_DST REGISTER 3011	ADDRESS OF RLD_SRC REGISTER 3006	←	←
QNT REGISTER 3015	ARBITRARY	BYTE1	BYTE2
RLD_QNT REGISTER 3016	5	←	←
CTL REGISTER 3020	ENB BIT=1 RLD_ENB BIT=1	ENB BIT=1 RLD_ENB BIT=1	ENB BIT=1 RLD_ENB BIT=0

Title: DATA PROCESSING CONTROL
APPARATUS AND DMA CONTROLLER
Inventor: MIURA, et al.
Appln. No. : Unknown
Docket No.: 103213-00057

FIG.22

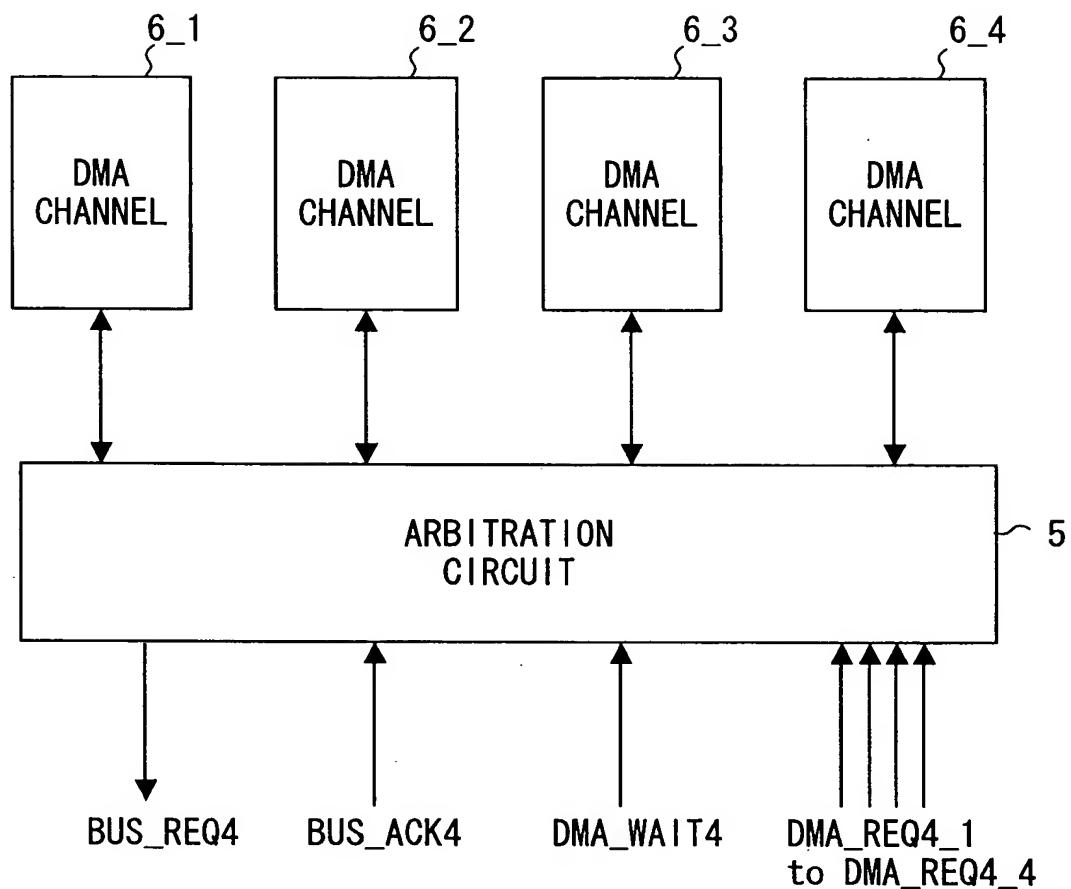


FIG.23

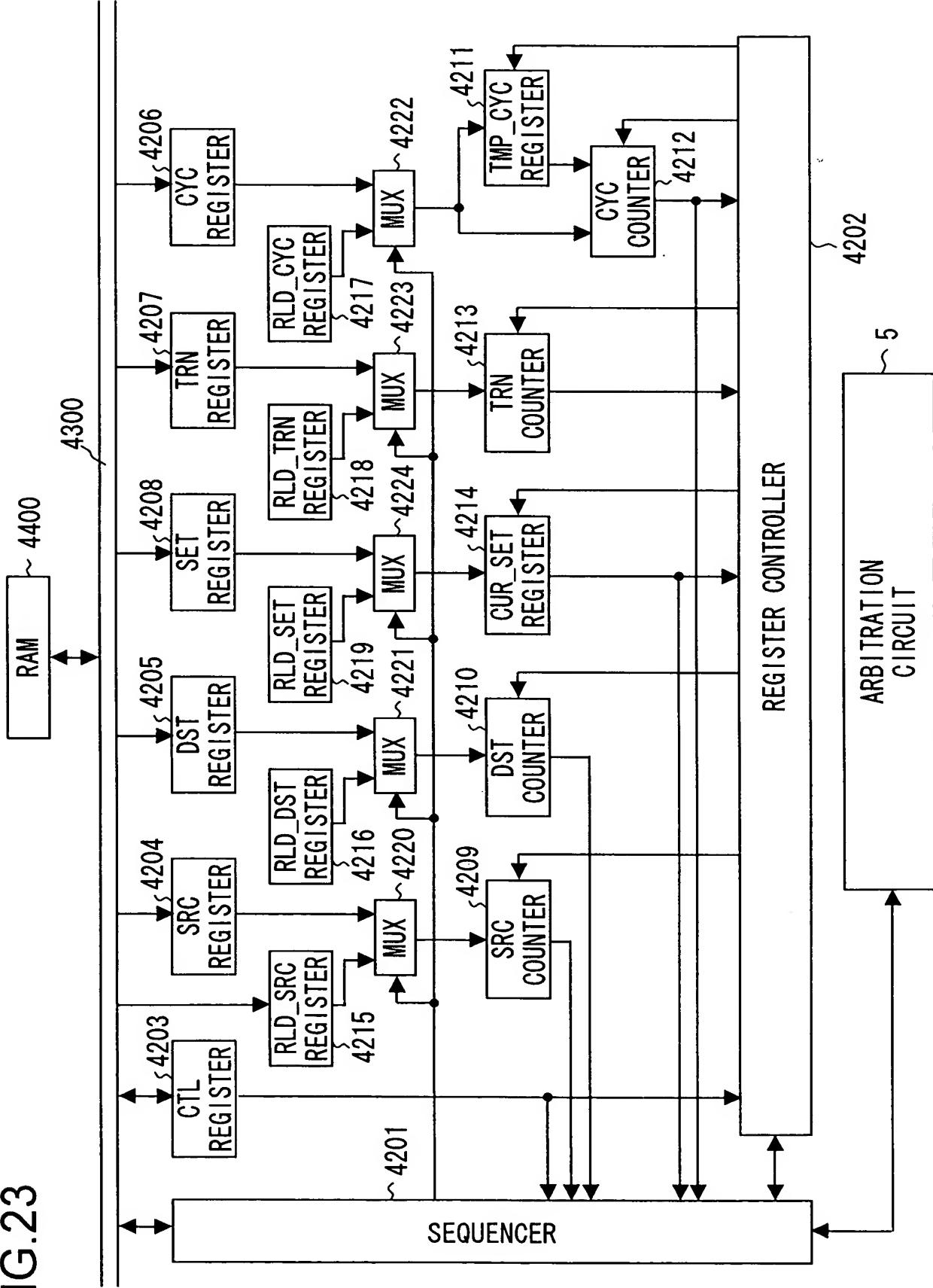


FIG.24

ADDRESS (Hex)	CONTENTS OF DATA
⋮	⋮
20000000-20000003	START ADDRESS (20007774) IN RAM 4400 WHERE INFORMATION NEEDED FOR 2ND DMA TRANSFER SESSION IS STORED
20000004-20000007	INFORMATION INDICATING START ADDRESS OF SOURCE IN 1ST DMA TRANSFER SESSION
20000008-2000000B	INFORMATION INDICATING START ADDRESS OF DESTINATION IN 1ST DMA TRANSFER SESSION
2000000C-2000000D	INFORMATION INDICATING NUMBER OF CYCLES INVOLVED IN ONE DMA TRANSFER SESSION IN 1ST DMA TRANSFER SESSION
2000000E-2000000F	INFORMATION INDICATING NUMBER OF DMA TRANSFER SESSIONS TO BE EXECUTED IN 1ST DMA TRANSFER SESSION
20000010-20000011	OTHER INFORMATION RELATING TO 1ST DMA TRANSFER SESSION
20000012	CONTROL INFORMATION RELATING TO 1ST DMA TRANSFER SESSION $S/W_START = 0$ $MOD[1, 0] = [1, 1]$
⋮	⋮
20007774-20007777	START ADDRESS (ARBITRARY) IN RAM 4400 WHERE INFORMATION NEEDED FOR 3RD DMA TRANSFER SESSION IS STORED
20007778-2000777B	INFORMATION INDICATING START ADDRESS OF SOURCE IN 2ND DMA TRANSFER SESSION
2000777C-2000777F	INFORMATION INDICATING START ADDRESS OF DESTINATION IN 2ND DMA TRANSFER SESSION
20007780-20007781	INFORMATION INDICATING NUMBER OF CYCLES INVOLVED IN ONE DMA TRANSFER SESSION IN 2ND DMA TRANSFER SESSION
20007782-20007783	INFORMATION INDICATING NUMBER OF DMA TRANSFER SESSIONS TO BE EXECUTED IN 2ND DMA TRANSFER SESSION
20007784-20007785	OTHER INFORMATION RELATING TO 2ND DMA TRANSFER SESSION
20007786	CONTROL INFORMATION RELATING TO 2ND DMA TRANSFER SESSION $S/W_START = 0$ $MOD[1, 0] = [1, 0]$
⋮	⋮

FIG.25

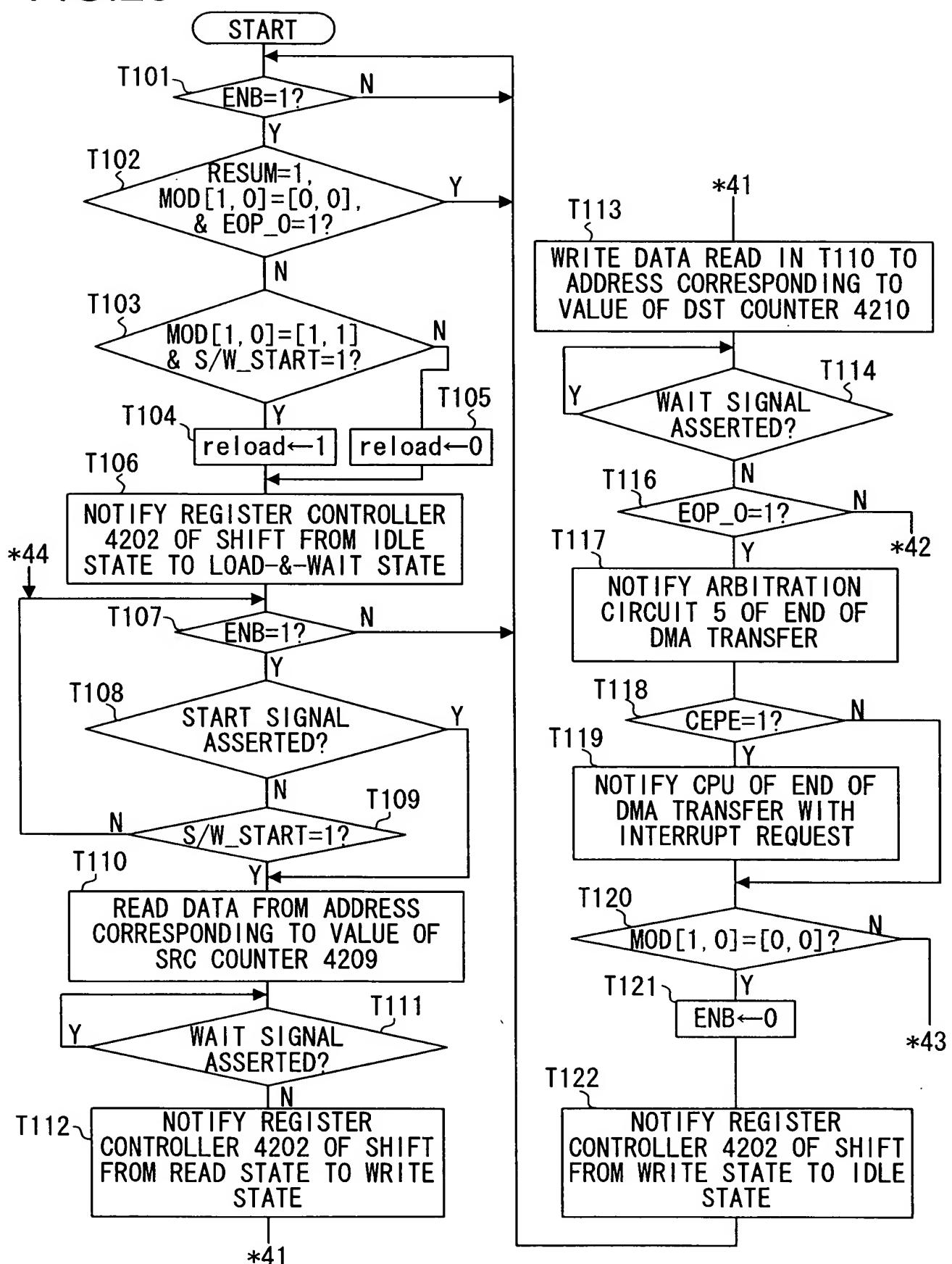


FIG.26

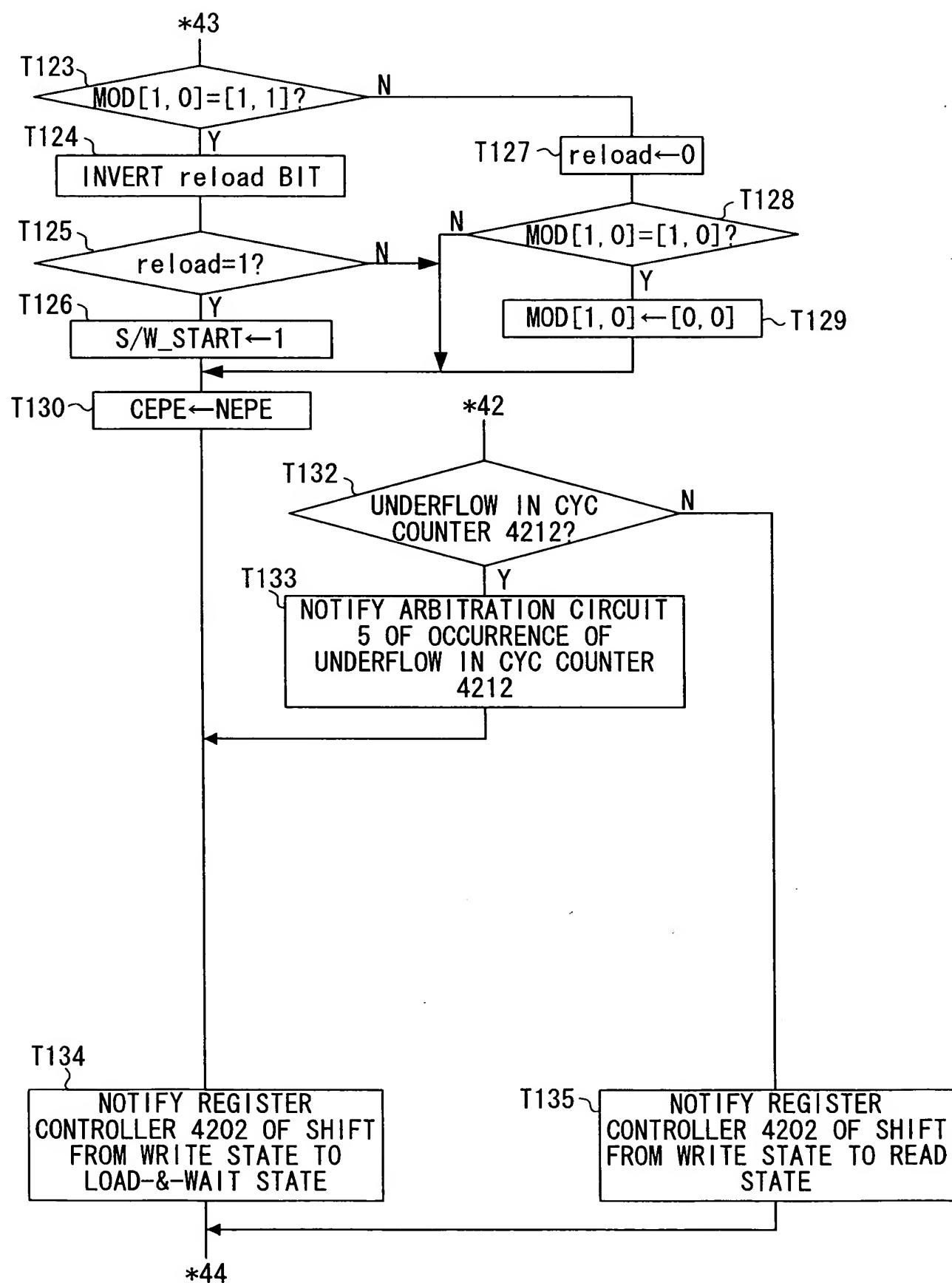


FIG.27

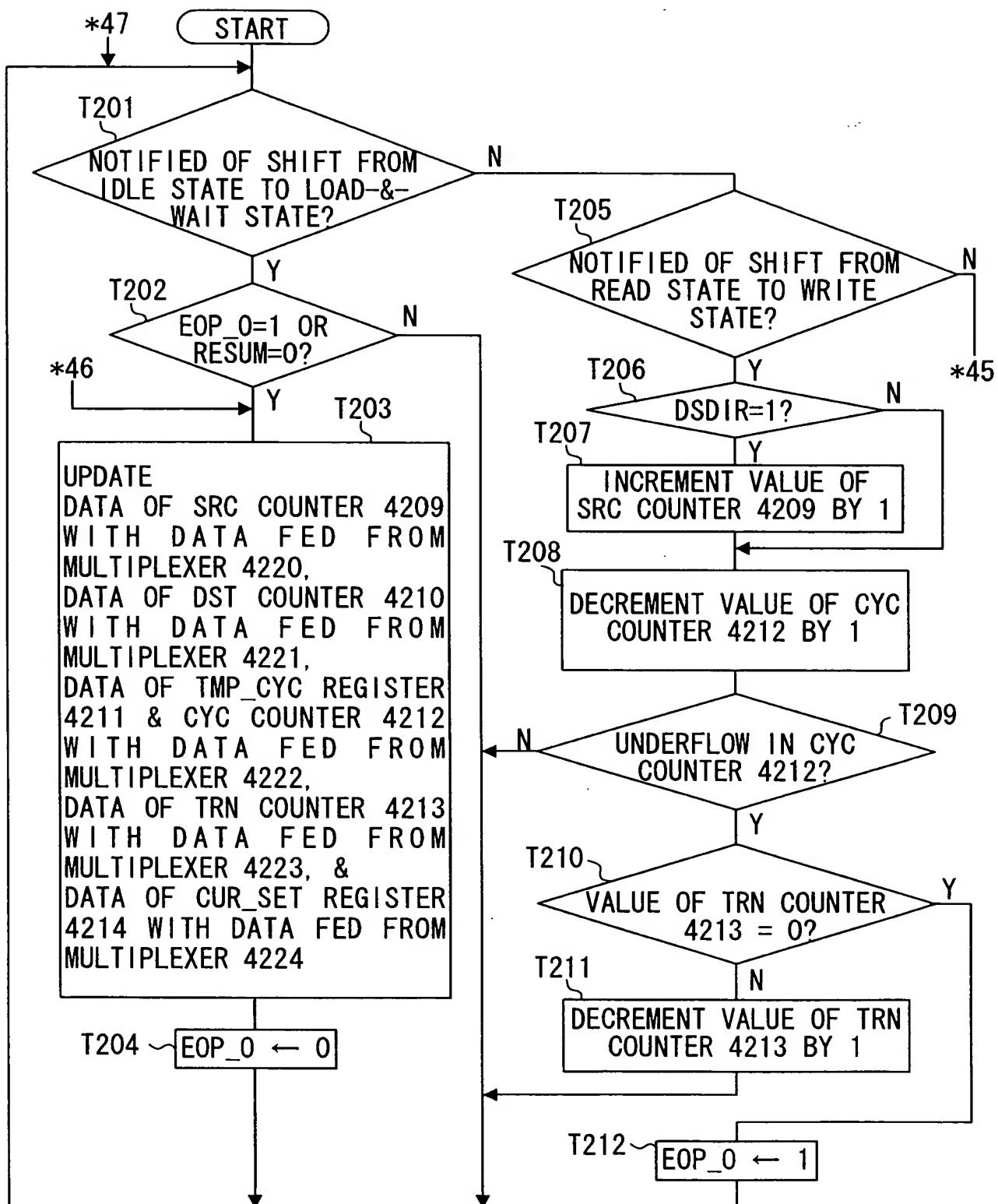


FIG.28

